Electronic Version
Stylesheet Version v1.1.1

METHOD FOR FABRICATING INTEGRATED CIRCUITS HAVING BOTH HIGH VOLTAGE AND LOW VOLTAGE DEVICES

Abstract

A high-voltage semiconductor MOS process that is fully compatible with low-voltage MOS process is provided. The high-voltage N/P well are implanted into the substrate prior to the definition of active areas. The channel stop doping regions are formed after the formation of field oxide layers, thus avoiding lateral diffusion of the channel stop doping regions. In addition, the grade drive-in process used to activate the grade doping regions in the high-voltage device area and the gate oxide growth of the high-voltage devices are performed simultaneously.